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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,652	01/18/2002	Ronalf Kramer	1406/36	5317

25297 7590 08/25/2004

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,652	KRAMER, RONALF	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-11, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomita (U. S. PAT. 5,936,429).

In claim 1, Tomita teaches all claimed features in Figs. 1 & 7, a circuit for generating a single asynchronous signal pulse at an output of an integrated circuit, the circuit comprising: an integrated circuit comprising a push-pull driving circuit (28, 30) having a first and second transistor (30, 28) including control terminals (gate terminals) being independently controlled by different control pulses (S3, S4) between a first and second supply potential (Vdd and ground), and a centre tap (32) connected with an output terminal (32) of the integrated circuit; and a single resistor (16) being externally coupled with the output terminal of the integrated circuit and being of a pull-up (as shown) or pull-down type, wherein the type of the resistor determines, by application of a first control pulse (S3) on the control terminal of the second transistor (28) and then a second control pulse (S4) on the control terminal of the first transistor (30), whether a single positive (leading edge) or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal; wherein a waiting time (see timing diagram in Fig. 7) is provided between the first

control pulse and the second control pulse such that the two pulses do not overlap (S3 and S4 do not overlap, as shown in the timing diagram in Fig. 7).

In claim 3, Tomita further teaches the circuit of claim 1 wherein one of the two control pulses is generated from the other of the two control pulses by an inverter delay device (22).

In claim 4, Tomita further teaches the circuit of claim 1 wherein the first transistor is a P-channel MOS transistor and the second transistor is an N-channel MOS transistor (as shown in Fig. 1), the control connection of the first transistor being inverted (S4).

In claim 5, Tomita further teaches the circuit of claim 4, wherein the first transistor (30) and the second transistor (28) form a CMOS inverter (as shown) with independent control gate connections (separate gate electrodes controlled by S4 & S3).

In claim 15, Tomita further teaches the circuit of claim 1 wherein the first and the second transistors (30, 28) include a source and drain, the drain of the first transistor being connected to the drain of second transistor (as shown in Fig. 1), the source of the first transistor being connected to the first power potential (Vdd), and the source of the second transistor being connected to the second supply potential (ground).

In claim 6, Tomita teaches all claimed features in Figs. 1 & 7, a circuit for generating a negative signal pulse in response to receiving a sequence of a positive and (S3) negative control pulse (S4), the circuit comprising: a first transistor (30) including a control terminal (a gate terminal for 30) and a load path (between Vdd and node 32) connected between an output terminal (32) and a first supply potential (Vdd) for receiving a negative control pulse (S4) at the control terminal; a second transistor

(28) including a control terminal (a gate terminal for 28) and a load path (between node 32 and ground) connected between the output terminal (32) and a second supply potential (ground) having a potential less than the first supply potential for receiving a positive control pulse (S3) at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse, wherein the first and second control terminals are independently controllable (as shown in Fig. 1 and timing diagram of Fig. 7); and a pull-up resistor (16) connected between the first supply potential (Vt; col. 3, lines 21-24) and the output terminal (32) for generating the negative signal pulse (S5) at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses (S4, S3).

In claim 7, Tomita further teaches all claimed features the circuit of claim 6 in Figs. 1 & 7, wherein a waiting time (a delay) is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap (S3 and S4 do not overlap, as shown in the timing diagram in Fig. 7).

In claim 8, Tomita further teaches wherein one of the two control pulses is generated from the other of the two control pulses by an inverter delay device (22).

In claim 16, Tomita further teaches all claimed features the circuit of claim 6 in Figs. 1 & 7, wherein the first and the second transistors (30, 28) include a source and drain, the drain of the first and second transistors being connected to the output terminal (32), the source of the first transistor being connected to the first supply potential (Vdd), and the source of the second transistor being connected to the second supply potential (ground).

Claims 9-11 and 17 correspond to detailed circuitry already discussed similarly with regard to claims 6-8 and 16.

Claims 12-14 are not entered.

Response to Arguments

3. Applicant's arguments with respect to claims 6 and 9 have been considered but are moot in view of the new ground(s) of rejection.

The newly cited reference of Tomita '429 anticipates all claimed features of this instant application, as discussed above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER